

# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

PUBLICATION NUMBER : 63142832  
 PUBLICATION DATE : 15-06-88

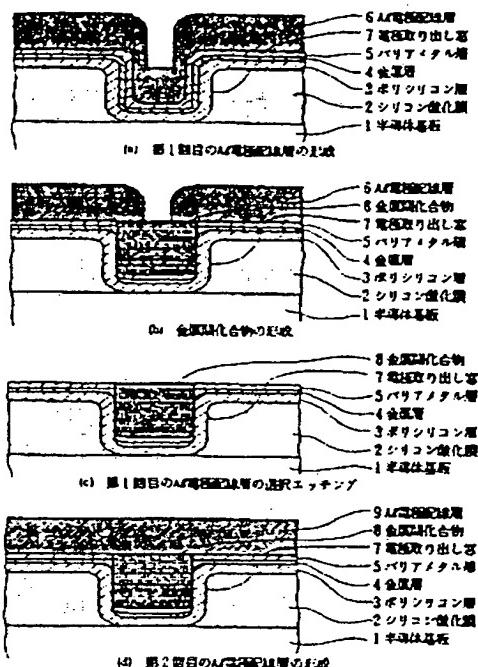
APPLICATION DATE : 05-12-86  
 APPLICATION NUMBER : 61290954

APPLICANT : FUJITSU LTD;

INVENTOR : BOKU KEIKOU; MIHARA SATOSHI;

INT.CL. : H01L 21/88 H01L 21/28

TITLE : MANUFACTURE OF  
 SEMICONDUCTOR DEVICE



**ABSTRACT :** PURPOSE: To form a flat surface in which the irregular thickness of an aluminum electrode wiring layer or the improper disconnection of wirings can be prevented by forming an intermetallic compound of a barrier metal layer and the aluminum electrode wiring layer in an electrode leading window by annealing to eliminate the stepwise difference from the surface of the barrier metal layer.  
 CONSTITUTION: A polysilicon layer 3, a metal layer 4, and a barrier metal layer 5 are sequentially laminated in an electrode leading window 7 formed on a silicon oxide film 2 formed on a semiconductor substrate 1. When an annealing is executed, only the perpendicular surface of a barrier metal layer 5 made of TiN is varied in quality to be reacted with the aluminum of an aluminum electrode wiring layer 6 to form an intermetallic compound 8 made of aluminum titanium (AlTi), thereby filling a space surrounded by the sidewall of the layer 3 of the window 7. The first aluminum electrode wiring layer 6 is removed by selective etching to form the continuous surfaces of the layer 5 and the compound 8. A second aluminum electrode wiring layer 9 is eventually formed on the layer 5 and the compound 8 formed flatly.

COPYRIGHT: (C) JPO